REMARKS

I. Status of the Application

Claims 1-22 are pending in this application. In the May 8, 2003 Office Action, the Examiner:

1. Objected to the Drawings as allegedly failing to comply with 37 C.F.R. 1.84(p)(4) and (p)(5);

2. Objected to claim 4 for informalities;

3. Rejected claims 1, 4, 6, 7, 9, 13-17 and 20-22 under 35 U.S.C. § 102(e) as allegedly being anticipated by U.S. Patent No. 4,144,141 to Travis, (hereinafter "Travis").

4. Rejected claims 2, 3, 10-12, 18 and 19 under 35 U.S.C. § 103(a) as allegedly being obvious over Travis;

5. Rejected claims 5 and 14 under 35 U.S.C. § 103(a) as allegedly being obvious over Travis in view of U.S. Patent No. 4,902,964 to Szabela (hereinafter "Szabela");

6. Rejected claim 8 under 35 U.S.C. § 103(a) as allegedly being obvious over Travis in view of U.S. Patent No. 6,429,785 to Griffin et al. (hereinafter "Griffin").

Applicant respectfully traverses the rejections of the claims and respectfully request reconsideration of the pending claims in view of the following remarks.

II. The Objections to the Drawings Have Been Addressed

The Examiner objected to the drawings because the reference number 116 had been used in Fig. 1 to designate both the communication circuit and the multiplexer. The Examiner further objected to the drawings because Fig. 1 showed the Precision Time Signal Receiver without the reference number 103, as is used in the specification.

In this amendment, Applicant has amended Fig. 1 to include the reference number 103 to designate the Precision Time Signal Receiver, and has further changed the reference number of the Communication Circuit from "116" to "114". It is noted that the last two lines of page 13 of the application as filed refer to the communication circuit with the reference number 114.

Because the amendments to Fig. 1 address the objections to the drawings raised by the Examiner in the May 8, 2003 office action, it is respectfully submitted that those objections should be withdrawn.

III. The Objection to Claim 4 Has Been Addressed

The Applicant has amended claim 4 in response to the Examiner's objection. In particular, the Applicant has deleted the second instance of the word "signal". Because the amendment to claim 4 addresses the objection raised by the Examiner in the May 8, 2003 office action, it is respectfully submitted that the objection to claim 4 should be withdrawn.

IV. The Anticipation Rejections are in Error

The Examiner has rejected claims 1, 4, 6, 7, 9, 13-17 and 20-22 under 35 U.S.C. § 102(e) as allegedly being anticipated by Travis. As will be discussed below, Travis fails to disclose each and every element of any of claims 1, 4, 6, 7, 9, 13-17 and 20-22. As a result, the anticipation rejection of those claims should be withdrawn.

A. The Present Invention of Claim 1

Claim 1 is directed to an apparatus for generating precision clock information, comprising a source of power line timing information, a source of externally-generated precision time information, and a timing circuit. The timing circuit is coupled to the source of externally-generated precision time information to receive a precision time information therefrom, and is operable to generate clock information based on the precision time signal. The timing circuit is further operable to generate clock information based on the power line timing information.

Thus, the above invention has the ability to maintain highly accurate timing information because clock information is derived from multiple sources, namely the power line and an external precision time source.

B. Travis

Travis is directed to a system for transmitting digital information from a remote station to a central station. The system is primarily directed to transmitting numbers using synchronized counters. The transmitted numbers may be representative of energy consumption. The system involves sending a start pulse from a first station to a second

station. The first station methodically counts down from a number representative of the number to be transmitted, using the standard AC waveform as the clock input to the counter. The second station receives the start pulse and starts incrementing an up-counter at the same time, also using the AC waveform as its clock input to its counter. When the transmitting station has counted down to zero, it sends a stop pulse to the receiving station. The receiving station receives the stop pulse and stops its up-counter. The up-counter at the receiving station should now contain the value that was previously in the transmitting station's down-counter. Thus, the data from the transmitting station's down-counter has been "transmitted".

C. Travis Fails to Teach or Suggest a Timing Circuit as Claimed

Travis fails to teach or suggest a timing circuit "operable to generate clock information based on the precision time signal [and] operable to generate clock information based on the power line timing information", where the precision time signal is obtained from a source of externally-generated precision time information, as called for in claim 1.

As will be discussed below in further detail, all clock information within Travis is derived solely from the AC power line, and not from any externally-generated precision time information. Indeed, it is not clear that Travis discloses any externally-generated precision time information at all.

In the May 8, 2003 office action, the Examiner alleged the following with respect to the precision time signal:

> With regard to claims 1 and 9, Travis teaches an apparatus for generating clock information for an electric meter comprising: a source of power line timing information (fig. 3, part 33a and col. 5, lines 36-42), a source of externally-generated precision time information (fig. 3, parts 30-33 and col. 5, lines 17-23), and a timing circuit coupled to the source of precision time information to receive a precision time signal (fig. 3, part 33), the timing circuit operable to generate clocking information based on the precision time signal, the timing circuit further operable to generate clock information based on the power line timing information (col. 6, lines 1-5 and col. 9, lines 21-30).

(P.3)

Applicants disagree that the cited passages of Travis support the Examiner's characterization. In particular, col. 5, lines 17-23 of Travis do not in any way suggest a source of externally generated precision timing information. The cited portion of Travis is set forth below:

> The communication system of the present invention is a new communication system which combines two different signals in a single communication system for transmitting digital information. Digital radio transmission is used as the primary data transmission technique in order to take advantage of its reliability, speed and low cost. In order to overcome the limited data han. . .
> (Travis at col. 5, lines 17-23)

The above passage does not even remotely suggest a source of timing information, much less a source of externally-generated precision timing information.

The other source of support cited by the Examiner is Fig. 3, items 30-33. Items 30-33 of Fig. 3 clearly show a source of externally-generated *information*, which could conceivably be considered to be *timing information*. However, the information received in items 30-33 is not used by a timing circuit to generate clock information as claimed.

i. Part 33 is not a Timing Circuit that Generates Clock Information

In particular, the Examiner alleges that part 33 of Fig. 3 of Travis constitutes the claimed timing circuit, and cites portions of col. 6 and col. 9 to this end. (See quoted excerpt of May 8, 2003 office action, above). The "part 33" of Fig. 3 of Travis is not a

timing circuit and does not generate clock information.

The cited passages that allegedly support the Examiner's contention that "part 33" constitutes the claimed timing circuit are provided below:

> digital information. The requested digital information can only be gathered by the central station by combining the reference signal transmitted over the 60 cycle power lines with the start and stop signals or the marking signal transmitted by the radio waves. (Travis at Col. 6, lines 1-5)

> Fig. 11B. The digital encoder 16 receives the 120 clock pulse from the power supply and timing source 15 as well as an XTMT (transmit) pulse signal which is also generated by the power supply and timing source 15. The XTMT pulse signal generated by the power supply and timing source 15 is derived from the 60 hz frequency of the power distribution system. The central station and the remote stations of the present invention are connected together by these power lines in the power distribution system. (Travis at Col. 9, lines 21-30)

Neither of these passages explain how the item 33 constitutes a timing circuit at all, much less a timing circuit as claimed. Item 33 is a "remote address identifier logic circuit". (See Travis at col. 11, lines 52-59). This circuit is *not* a timing circuit, and certainly does not "generate clock information" of any kind. Instead, the remote address identifier logic circuit 33 of Travis determines whether the incoming signal is addressed to the remote station.

ii. The Only Timing Circuit of Travis Fails to Generate Clock Signals Using Precision Time Signals

The only timing circuit in Fig. 3 of Travis is the power supply and timing source 33a. This power supply and timing source 33a does indeed receive power line timing information, but receives *no other* timing information or signals. Specifically, the timing source 33a of Travis does not receive a *precision time signal* from a source of externally-generated precision time information.

Thus, *even if it is assumed that elements 30-33 of Fig. 3 receive precision time*

information, those such precision time information is never received or used by the power supply and timing source 33a. As a consequence, the *only* timing circuit of Fig. 3, the timing source 33a, does not constitute the claimed timing circuit of claim 1.

It is completely understandable that Travis does not include the timing circuit as claimed. Travis is directed to completely different problems than those which the claimed invention is intended to solve. In particular, the claimed invention is intended to provide a more reliable and accurate time source for maintaining a more precise clock (e.g. a calendar clock used for time of use or demand metering) within the meter. (See Application at pp.2-4). To this end, an externally-generated precision time signal *and* the normally-accurate line voltage signal are used by the invention to generate clock information. This provides potential redundancy of accurate time sources, and/or a method of adjusting for inaccuracies of the line voltage signal.

Travis, by contrast, is completely unconcerned with maintaining or correcting internal clock information. Travis assumes that the line voltage signal alone is accurate enough. Whatever other "timing information" is received by the Travis device does not alter or substitute for the line voltage timing information. The Travis circuit does and can not provide redundancy in the event of a power line signal interruption nor can it adjust its internal clock using external information.

As a consequence, Travis fails to disclose or suggest at least the claimed timing circuit that is "operable to generate clock information based on the precision time signal [and] operable to generate clock information based on the power line timing information", as called for in claim 1. Because Travis fails to teach or disclose every element of claim 1, it is respectfully submitted that the rejection of claim 1 is in error and

should be withdrawn.

D. Claims 4, 6 and 7

Claims 4, 6 and 7 all stand rejected as allegedly being anticipated by Travis. Claims 4, 6 and 7 all depend from and incorporate all of the limitations of claim 1. Accordingly, for at least the same reasons as those discussed above in connection with claim 1, it is respectfully submitted that the rejections of claims 4, 6 and 7 are in error and should be withdrawn.

E. Claim 9

Claim 9 also stands rejected as being allegedly anticipated by Travis. Claim 9 is a method claim that recites steps of "generating clock information based on the precision time signal" and "generating clock information based on the power line timing information". Travis fails to disclose the combination of these steps.

As discussed above, the only device that generates clock information in Travis is the power supply and timing source 33a. While the timing source 33a of Travis does generate clock information based on power line timing information, it does *not* receive any other externally-generated precision time information. Because the timing source 33a does not even receive externally-generated precision time information (other than the power line timing information), the timing source 33a cannot perform both steps of "generating clock information based on the precision time signal" and "generating clock information based on the power line timing information".

Because Travis fails to teach or disclose every element of claim 9, it is

respectfully submitted that the rejection of claim 9 is in error and should be withdrawn.

F. Claims 13, 15 and 16

Claims 13, 15 and 16 all stand rejected as allegedly being anticipated by Travis. Claims 13, 15 and 16 all depend from and incorporate all of the limitations of claim 9. Accordingly, for at least the same reasons as those discussed above in connection with claim 9, it is respectfully submitted that the rejections of claims 13, 15 and 16 are in error and should be withdrawn.

G. Claim 17

Claim 17 stands rejected as allegedly being anticipated by Travis. Claim 17 is directed to a meter that includes, among other things, a timing circuit substantially identical to that of claim 1. As discussed above in connection with claim 1, Travis fails to teach or suggest the timing circuit as claimed. Accordingly, for at least the same reasons as those discussed above in connection with claim 1, it is respectfully submitted that the rejection of claim 17 is in error and should be withdrawn.

In addition, the Examiner has not specifically alleged whether or how Travis teaches "a memory operable to store at least some energy consumption data and a time record associated therewith, the time record generated in part using the clock information". In the May 8, 2003 office action, the Examiner alleged that a memory is taught by Travis at col. 11, lines 52-56. (Office Action at p.4). The cited portion of the Travis discusses an up-counter that is located within the "remote address identifier logic circuit 33", and states that it "stores the address and instruction corresponding to the start

and mark pulses". It is submitted that "address and instruction" does not constitute the claimed "energy consumption data and a time record associated therewith", as called for in claim 17.

Accordingly, for reasons independent to those applicable to claim 1, it is respectfully submitted that the rejection of claim 17 is in error and should be withdrawn.

H. Claims 20-22

Claims 20-22 all stand rejected as allegedly being anticipated by Travis. Claims 20-22 all depend from and incorporate all of the limitations of claim 17. Accordingly, for at least the same reasons as those discussed above in connection with claim 17, it is respectfully submitted that the rejections of claims 20-22 are in error and should be withdrawn.

V. The Obviousness Rejections Should be Withdrawn

A. Claims 2-3, 10-12, 18 and 19

Claims 2-3, 10-12, 18 and 19 have been rejected as allegedly obvious over Travis. As an initial matter, claims 2-3, 10-12, 18 and 19 all depend from one of claims 1, 9 or 17. As discussed above, Travis fails to teach all of the limitations of claims 1, 9 or 17. The proposed modification of Travis suggested by the Examiner in the rejection of claims 2-3, 10-12, 18 and 19 does not overcome the deficiencies of Travis with respect to claims 1, 9 and 17. Accordingly, for at least the same reasons as those set forth above in connection with claims 1, 9 and 17, it is respectfully submitted that the rejections of claims 2-3, 10-12, 18 and 19 are in error and should be withdrawn.

In addition, claims 2-3, 10-12, 18 and 19 all include limitations in which allows "clock information" to be based on *one of* the power line timing information or the precision time signal in the event that *the other* of the power line timing information or the precision time signal is unavailable. In other words, claims 2-3, 10-12, 18 and 19 disclose an *added function* of *redundancy.*

The Examiner admitted that Travis failed to teach the limitations of claims 2-3, 10-12, 18 and 19. (May 8, 2003 office action at p.5). However, the Examiner alleged that it would have been obvious to *add this capability* because "it has been held, however, that omission of an element and its function in a combination where the remaining elements perform the same function as before involves only routine skill in the art". (Citing In re Karlsen, 136 USPQ 184 (CCPA 19963)).

Claims 2-3, 10-12, 18 and 19 do not "omit an element and its function" from the prior art of Travis, as was the case of the claim at issue in In re Karlsen. Claims 2-3, 10-12, 18 and 19 *add* a function, that of being able to generate clock information when the other source of timing information is unavailable. This added function is a form of *redundancy.*

By contrast, the applicant in In re Karlsen attempted to argue patentability of a claim based on the limitation "an unobstructed interior space". The "unobstructed interior space" was not present in the prior art, but could be achieved by merely removing a superfluous wire mesh screen from the prior art device. 136 USPQ at 185. The CCPA held that the removal of the mesh screen (and its function) from the prior art device, which would then arrive at the claimed invention, did not amount to a nonobvious improvement.

In the instant case, there is nothing that can be *removed* from Travis to arrive at the invention of claims 2-3, 10-12, 18 and 19. Those claims *add* the function of redundancy. Travis would need new circuitry, not the removal of devices and functions, in order to add the redundancy of claims 2-3, 10-12, 18 and 19. Thus, the reasoning of In re Karlson does not support an obviousness rejection in this Application.

Moreover, Travis neither suggests nor contemplates the need for redundancy. Indeed, removal of the AC line voltage signal from Travis would render the communication circuit completely *inoperable*. Accordingly, it is respectfully submitted that the rejection of claims 2-3, 10-12, 18 and 19 are in error for reasons independent of those set forth above in connection with claims 1, 9 and 17.

B. Claims 5 and 14

Claims 5 and 14 have been rejected as allegedly obvious over Travis in view of Szabela. As an initial matter, claims 5 and 14 depend from claims 1 and 9, respectively. As discussed above, Travis fails to teach all of the limitations of either of claims 1 or 9. The proposed modification of Travis proposed by the Examiner in the rejection of claims 5 and 14 does not overcome the deficiencies of Travis with respect to claims 1 or 9. Accordingly, for at least the same reasons as those set forth above in connection with claims 1 and 9, it is respectfully submitted that the rejection of claims 5 and 14 is in error and should be withdrawn.

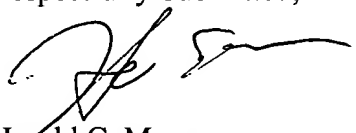
C. Claim 8

Claim 8 stands rejected as allegedly being obvious over Travis in view of Griffin. Claim 8 depends from and incorporates all the limitations of claim 1. As discussed above, Travis fails to teach all of the limitations of claim 1. The proposed modification of Travis proposed by the Examiner in the rejection of claim 8 does not overcome the deficiencies of Travis with respect to claim 1, respectively. Accordingly, for at least the same reasons as those set forth above in connection with claim 1, it is respectfully submitted that the rejection of claim 8 is in error and should be withdrawn.

VI. Conclusion

For all of the foregoing reasons, it is respectfully submitted the Applicant has made a patentable contribution to the art. Favorable reconsideration and allowance of this application is, therefore, respectfully requested.

Respectfully Submitted,



Harold C. Moore
Attorney for Applicant
Attorney Registration No. 37,892
Maginot, Moore & Bowman
Bank One Center/Tower
111 Monument Circle, Suite 3000
Indianapolis, Indiana 46204-5115
Telephone: (317) 638-2922